

## 700mA, 1.2MHz Synchronous Step-Up Converter

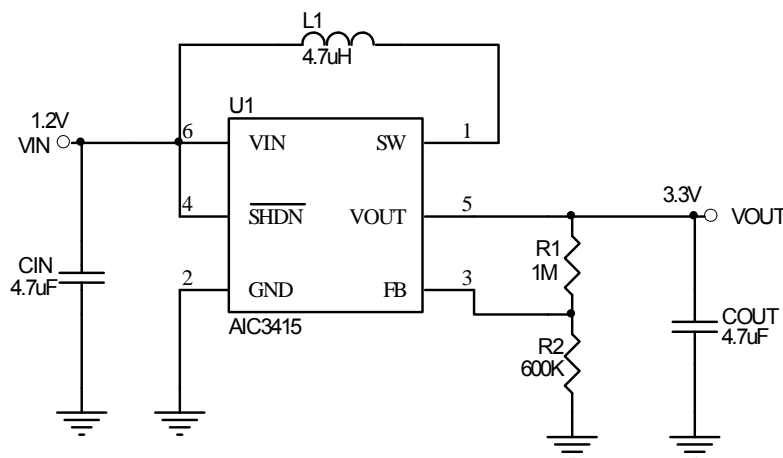
### FEATURES

- $V_{IN}$  Start Up Voltage: 0.9V
- Output Voltage Range: from 2.7V to 5.25V.
- Up to 94% Efficiency
- 1.2MHz Fixed Frequency Switching
- Built-in current mode compensation
- Built-in Protection: Over Current, Over Voltage, Over Temperature
- Optional Automatic PWM/PSM Version (AIC3415) and Forced PWM Version (AIC3415A).
- Logic Controlled Shutdown:  $< 1\mu A$
- Output Disconnect by Shutdown Function
- Built-in Soft Start
- Active Anti-ringing Control
- Small SOT-23-6 Package

### APPLICATIONS

- Single/Dual Cells Ni-Cd/Ni-Mh/Li-Lon Type Battery Operated Products
- Wireless Mice
- PDA
- Digital Still Cameras
- Portable Equipment

### TYPICAL APPLICATION CIRCUITS



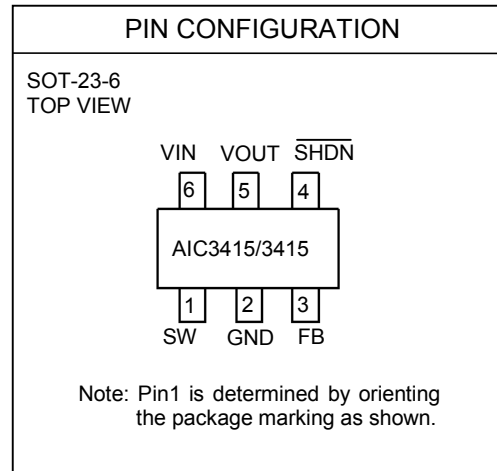
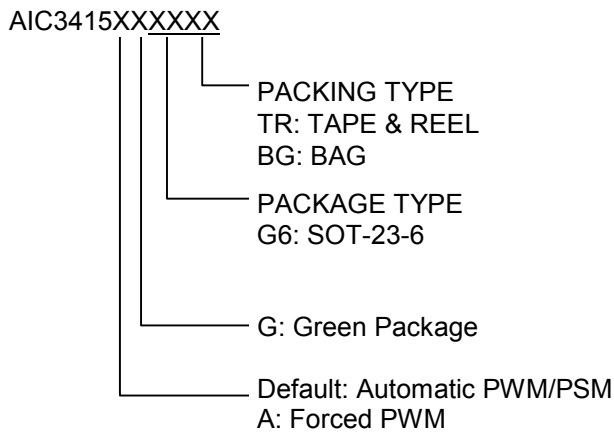
### DESCRIPTION

The AIC3415 is a synchronous step-up DC/DC converter.

There are two options for AIC3415: automatic PWM/PSM version (AIC3415), and forced PWM version (AIC3415A). The automatic PWM/PSM version enters PSM from PWM automatically when load decreases. The goal is to improve efficiency and reduce quiescent current; the forced PWM version keeps the same operating frequency even when it operates in light load. This guarantees low output ripple and noise. The AIC3415 provides a complete power supply solution for products powered by one or two Alkaline, Ni-Cd, Ni-MH or Li-Lon battery cells. It stays in operation with supply voltages down to 0.5V. The implemented boost converter uses an internal synchronous rectifier to obtain maximum efficiency.

A low-EMI mode is implemented to reduce ringing and in effect lower radiated electromagnetic energy when the converter enters the discontinuous conduction mode.

## ORDERING INFORMATION



Example: AIC3415GG6TR  
 → Automatic PWM/PSM  
 in SOT-23-6 Green Package and Tape & Reel  
 Packing Type  
 AIC3415AGG6TR  
 → Forced PWM  
 in SOT-23-6 Green Package and Tape & Reel  
 Packing Type

## ABSOLUTE MAXIMUM RATINGS

Pins Voltage: LX, FB, EN, OUT, VIN .....	-0.3 V to 6V
Operating Ambient Temperature Range $T_A$ .....	-40°C to 85°C
Operating Maximum Junction Temperature $T_J$ .....	150°C
Storage Temperature Range $T_{STG}$ .....	-65°C to 125°C
Lead Temperature (Soldering 10 Sec.) .....	260°C
Thermal Resistance (Junction to Case) .....	115°C/W
Thermal Resistance (Junction to Ambient) .....	250°C/W

(Assume no Ambient Airflow, no Heatsink)

**Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.**

**■ ELECTRICAL CHARACTERISTICS**

(Typical application circuit, and the ambient temperature=25°C,  $V_{IN}=1.2V$ ,  $V_{OUT}=3.3V$ , Unless otherwise specified) (Note1)

PARAMETER	TEST CONDITION	SYMBOL	MIN	TYP	MAX	UNIT
Output Voltage Range	$I_{OUT}=0A$	$V_{OUT}$	2.7		5.25	V
Minimum Start Up Voltage				0.9	1.1	V
Minimum Operation Voltage	Note2			0.5		V
Quiescent Current ( $V_{FB}>1.23V$ , Non-Switching)	AIC3415 only	$I_{Q0}$		40	60	$\mu A$
	AIC3415A only	$I_{Q0}$		250		$\mu A$
Shut Down Current (Oscillator no switching)	$\overline{SHDN}=0V$ , $V_{IN}=1.1V$	$I_{SD}$		0.3	1	$\mu A$
Feedback Voltage	$I_{OUT}=0$	$V_{FB}$	1.17	1.2	1.23	V
FB Input Leakage Current	$V_{FB}=1.3V$	$I_{FB}$		1	50	nA
Maximum Duty Cycle	$V_{FB}=1.15V$		80	88		%
Minimum Duty Cycle	$V_{FB}=1.3V$				0	%
Frequency			0.95	1.2	1.5	MHz
NMOS Switch Leakage	$V_{SW}=5V$			0.1	10	$\mu A$
PMOS Switch Leakage	$V_{SW}=5V$ , $V_{OUT}=0V$			0.1	10	$\mu A$
NMOS Switch On Resistance				350		m $\Omega$
PMOS Switch On Resistance				450		m $\Omega$
SHDN High Threshold Voltage			0.88			V
SHDN Low Threshold Voltage					0.25	V
SHDN Input Current	$\overline{SHDN}=5.25V$	$I_{SHDN}$		0.01	1.0	$\mu A$
NMOS Current Limit Setting			1.0	1.3		A
Over Temperature Protection				150		$^{\circ}C$
Over Temperature Hysteresis				25		$^{\circ}C$

Note 1: Specifications are production tested at  $T_A=25^{\circ}C$ . Specifications over the  $-40^{\circ}C$  to  $85^{\circ}C$  operating temperature range are assured by design, characterization and correlation with Statistical Quality Controls (SQC).

Note 2: Once the output is started, the IC is not dependant upon the  $V_{IN}$  supply.

**TYPICAL PERFORMANCE CHARACTERISTICS**

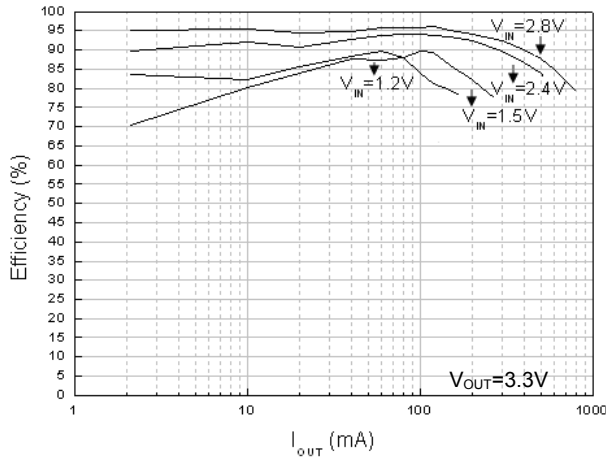


Fig. 1 Efficiency vs. Output Current

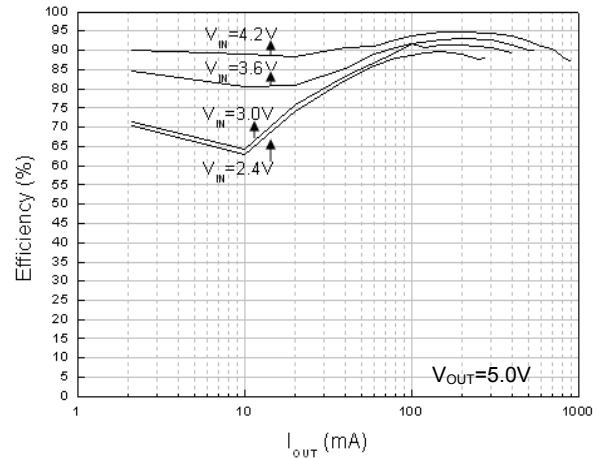


Fig. 2 Efficiency vs. Output Current

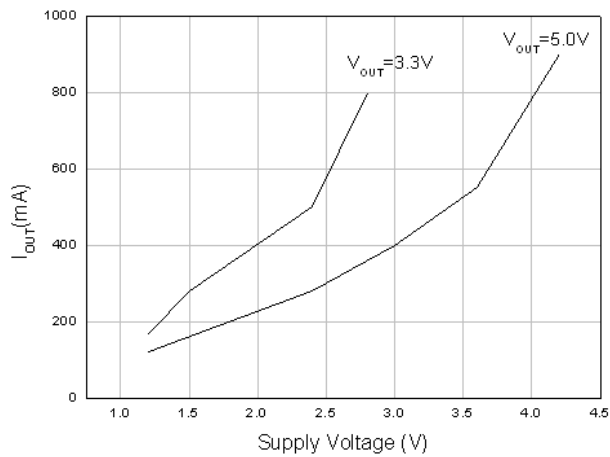


Fig. 3 Maximum Output Current vs. Supply Voltage

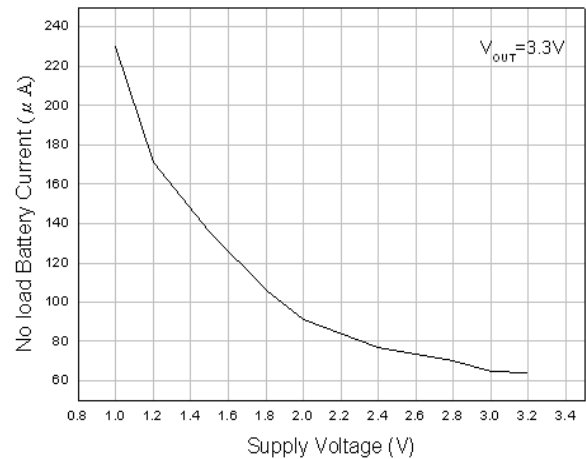


Fig. 4 No load Battery Current vs. Supply Voltage

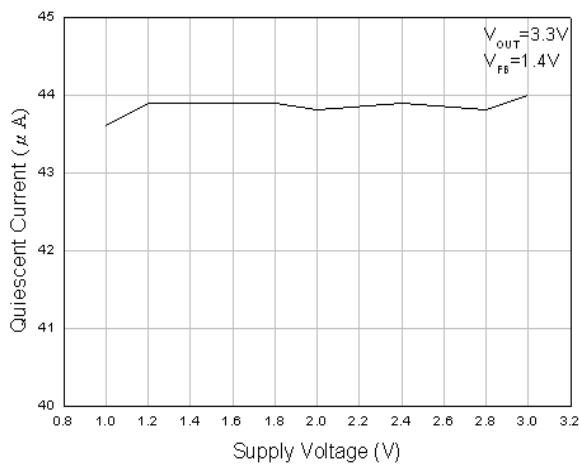


Fig. 5 Quiescent Current vs. Supply Voltage

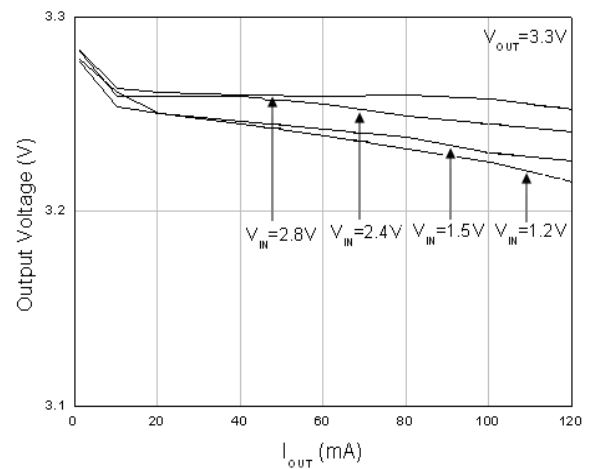


Fig. 6 Output Voltage vs. Output Current

**TYPICAL PERFORMANCE CHARACTERISTICS** (Continued)

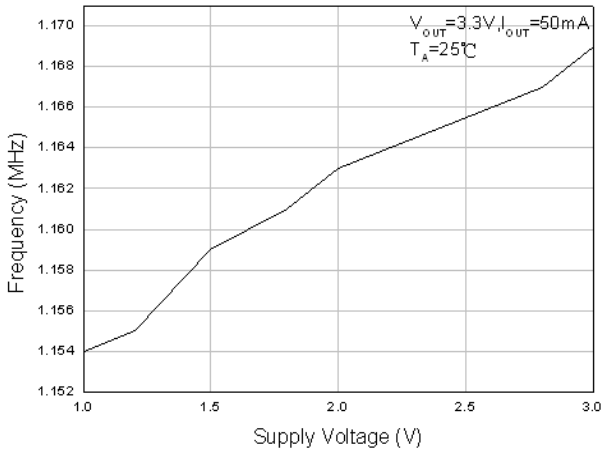


Fig. 7 Frequency vs. Supply Voltage

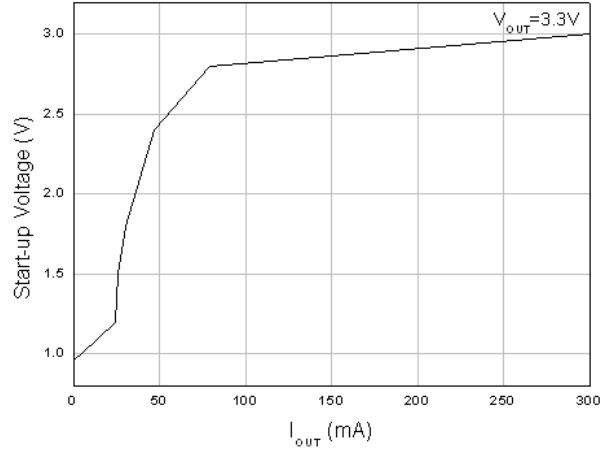


Fig. 8 Minimum Start-up Voltage vs. Output current

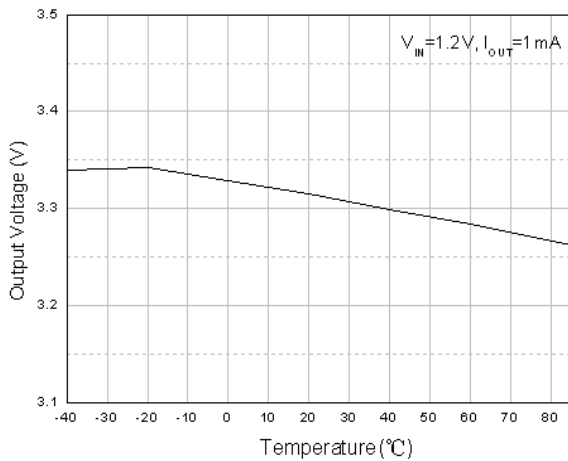


Fig. 9 Output Voltage vs. Temperature

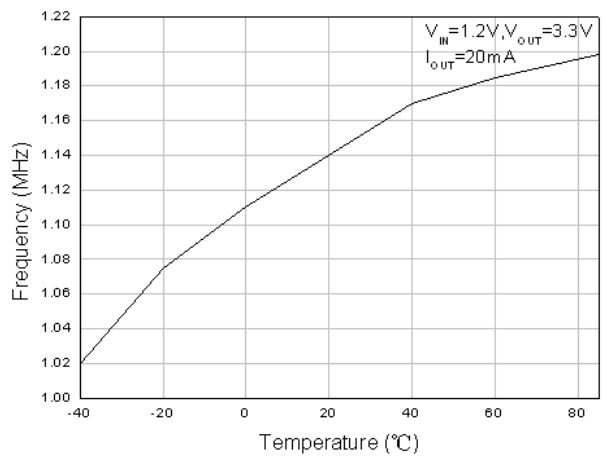


Fig. 10 Frequency vs. Temperature

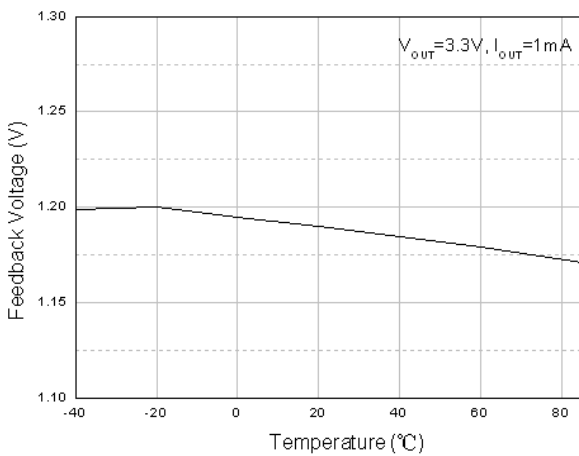


Fig. 11 Feedback Voltage vs. Temperature

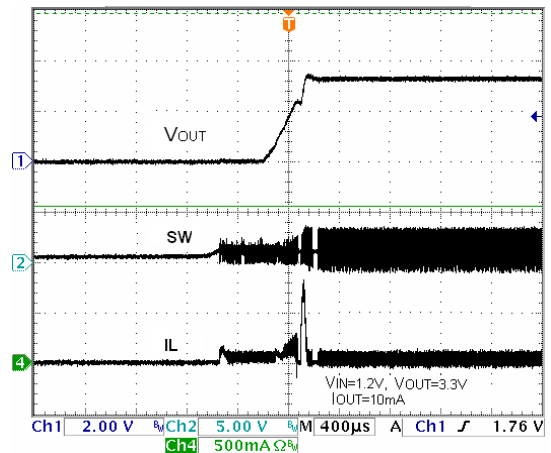


Fig. 12 Start-up Voltage Waveform

**TYPICAL PERFORMANCE CHARACTERISTICS** (Continued)

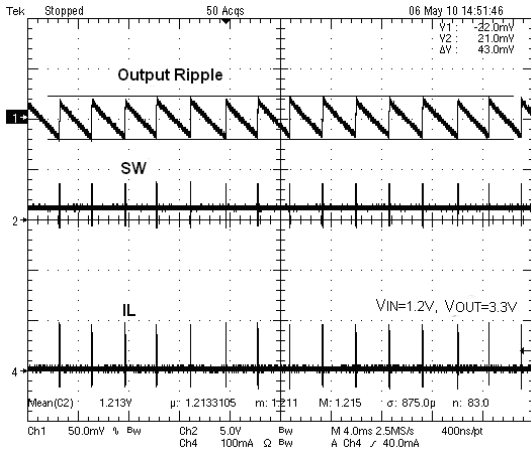


Fig. 13 PSM Mode Operation at  $I_{OUT}=0mA$

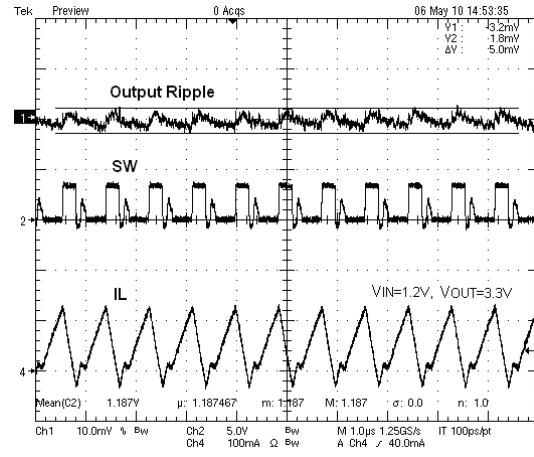


Fig. 14 Anti-Ringing Operation at  $I_{OUT}=10mA$

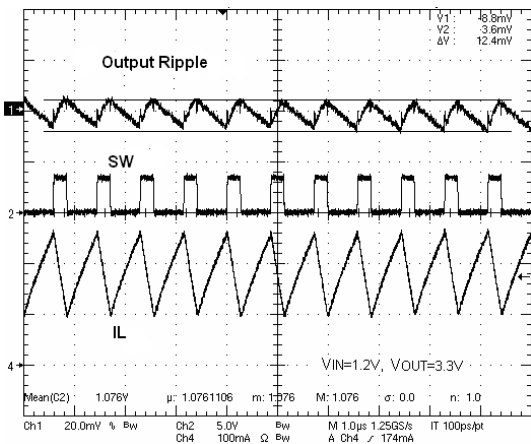


Fig. 15 CCM Switching Waveform at  $I_{OUT}=50mA$

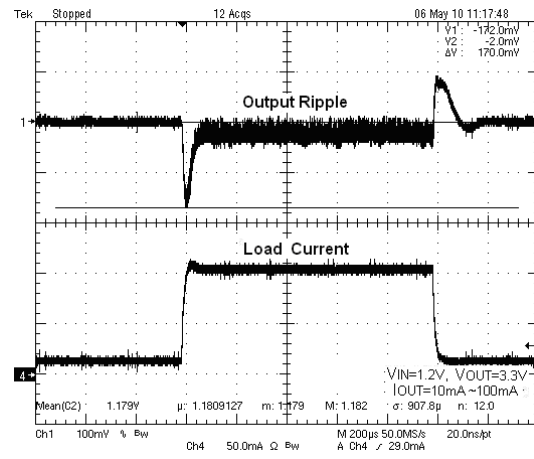


Fig. 16 Load Transient Response

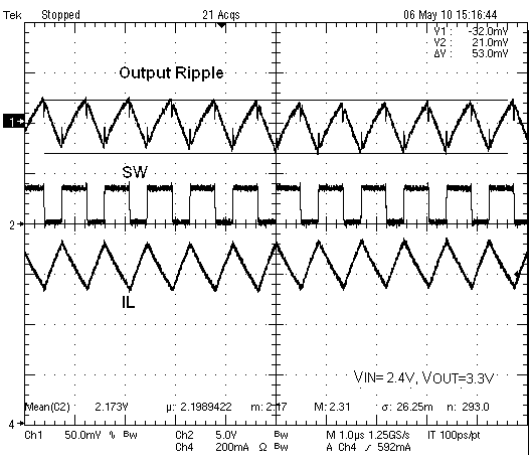


Fig. 17 CCM Switching Waveform at  $I_{OUT}=350mA$

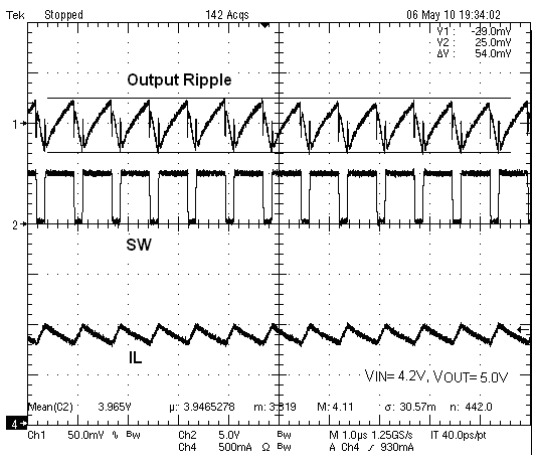
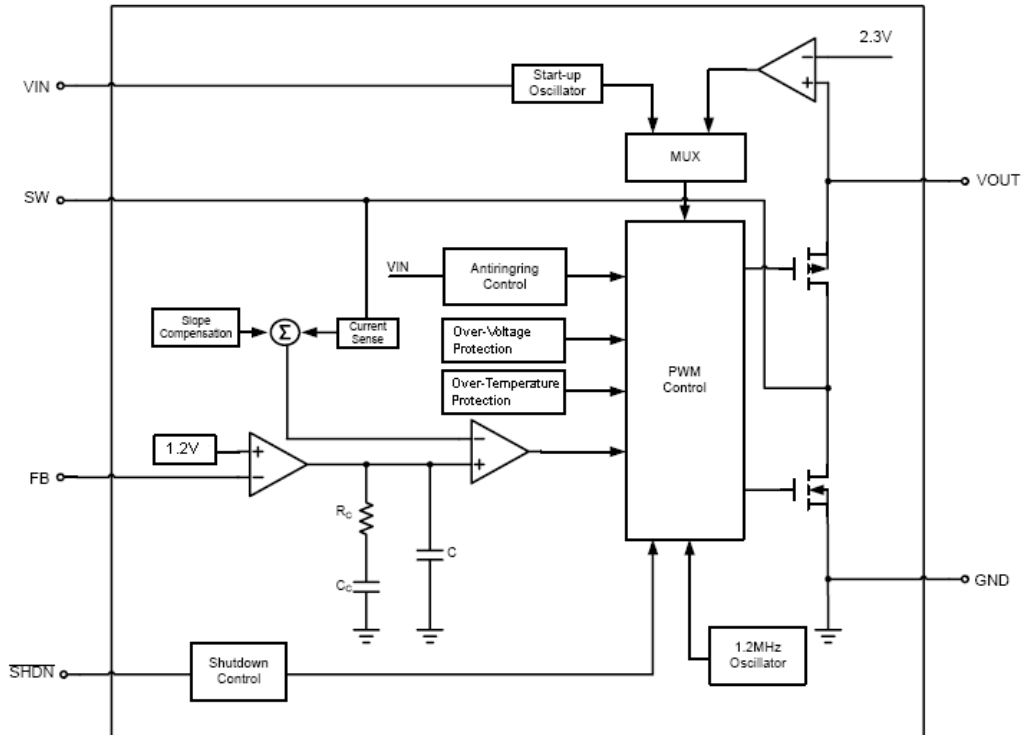


Fig. 18 CCM Switching Waveform at  $I_{OUT}=650mA$

## ■ BLOCK DIAGRAM



## ■ PIN DESCRIPTIONS

PIN 1: SW - Power Switch Pin. This pin is tied to the drains of the PMOS synchronous rectifier and the NMOS switch.

PIN 2: GND - I/O Control/logic ground.

PIN 3: FB - Output reference voltage is typically 1.2V

PIN 4:  $\overline{\text{SHDN}}$  - Shutdown Signal Input. Logic high enables the IC. Logic low disables the IC. Shutdown current is  $<1\mu\text{A}$ .

PIN 5: VOUT- Power Output Pin. This pin is tied to the source of the PMOS synchronous rectifier.

PIN 6: VIN - Power Supply Input. Must be closely decoupled to GND with a  $4.7\mu\text{F}$  or greater ceramic capacitor.

## ■ APPLICATION INFORMATION

The AIC3415 is a synchronous step-up DC-DC converter. It is based on a slope compensated current mode PWM control topology. It operates at a fixed frequency of 1.2MHz. At the beginning of each clock cycle, the main switch (NMOS) is turned on and the inductor current starts to ramp. After the maximum duty cycle or the sense current signal equals the error amplifier (EA) output, the main switch is turned off and the synchronous switch (PMOS) is turned on. The device can operate with an input voltage below 1V; the typical start-up voltage is 0.9V.

### Current Limit

The over current protection is to limit the switch current. The output Voltage will be dropped when over current is happened. The current limit amplifier will shut the N-MOS switch off once the current exceeds its threshold. The current amplifier delay to output is about 100 nS.

### Anti-Ringing Control

An anti-ringing circuitry is included to remove the high frequency ringing that appears on the SW pin when the inductor current goes to zero. In this case, a ringing on the SW pin is induced due to remaining energy stored in parasitic components of switch and inductor. The anti-ringing circuitry clamps the voltage internally to the battery voltage and therefore dampens this ringing.

### Zero Current Comparator

The zero current comparator monitors the inductor current to the output and shuts off the synchronous rectifier once the current is below 20 mA, This prevents the inductor current from reversing in polarity improving efficiency at light loads.

### Device Shutdown

When  $\overline{\text{SHDN}}$  is set logic high, the AIC3415 is put into active mode operation. If  $\overline{\text{SHDN}}$  is set logic low, the device is put into shutdown mode and consumes less than 1 $\mu$ A of current. At the shutdown mode, the synchronous switch will turn off and the output voltage of AIC3415 step-up converter will reduce to 0V. After start-up, the internal circuitry is supplied by V<sub>OUT</sub>, however, if shutdown mode is enabled, the internal circuitry will be supplied by the input source again.

### Adjustable Output Voltage

An external resistor divider is used to set the output voltage. The output voltage of the switching regulator (V<sub>OUT</sub>) is determined by the following equation:

$$V_{\text{OUT}} = V_{\text{FB}} \times \left( 1 + \frac{R_1}{R_2} \right)$$

Where V<sub>FB</sub> is 1.2V reference voltage.

### Input Inductor Selection

The inductor value determines the ripple current. The approximate ripple current and inductance value are measured by the following equations:

$$\Delta I_L = \frac{V_{\text{IN}} D}{L \times F_{\text{SW}}}$$

Where  $\Delta I_L$  = inductor ripple current

F<sub>SW</sub> = switch frequency

D = duty cycle, (V<sub>OUT</sub> - V<sub>IN</sub>) / V<sub>OUT</sub>

Where  $\Delta I_L$  is inductor ripple current, F<sub>SW</sub> is switch frequency and D is the duty cycle. Increasing the value of inductance will reduce the output ripple current and ripple voltage.

### Input Capacitor Selection

Surfaces mount 4.7 $\mu$ F or greater, X5R or X7R, ceramic



capacitor is suggested for the input capacitor. The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the AIC3415. Low ESR/ESL X7R and X5R ceramic capacitors are ideal for this function. To minimize stray inductance, the capacitor should be placed as close as possible to the IC. This keeps the high frequency content of the input current localized, minimizing EMI and input voltage ripple. Always examine the ceramic capacitor DC voltage coefficient characteristics to get the proper value.

### Output Capacitor Selection

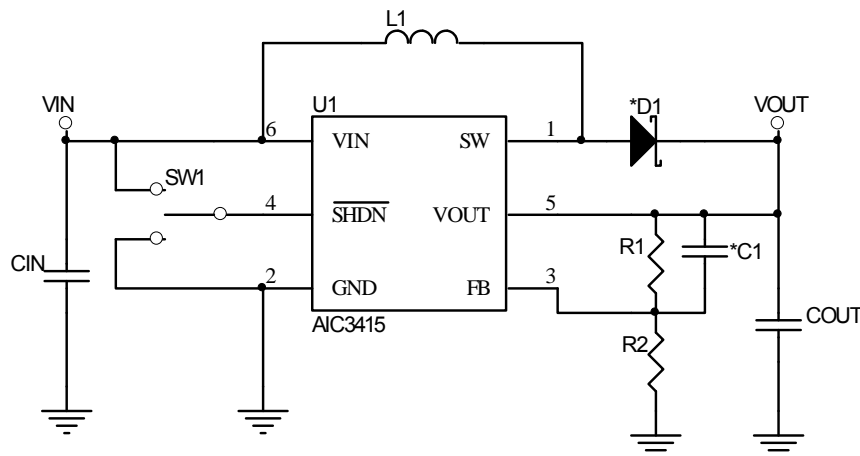
The output capacitor limits the output ripple and provides holdup during large load transitions. A 4.7 $\mu$ F to 10 $\mu$ F, X5R or X7R, ceramic capacitor is suggested for the output capacitor. Typically the recommended ca-

pacitor range provides sufficient bulk capacitance to stabilize the output voltage during large load transitions and has the low ESR and ESL characteristics necessary for low output voltage ripple.

### PCB Layout Guidance

The AIC3415 typically operates at 1.2MHz. This is a considerably high frequency for DC-DC converters. PCB layout is important to guarantee satisfactory performance. It is recommended to make traces of the power loop, especially where the switching node is involved, as short and wide as possible. First of all, the inductor, input and output capacitor should be as close as possible to the device. Feedback and shutdown circuits should avoid the proximity of large AC signals involving the power inductor and switching node.

## APPLICATION CIRCUITS

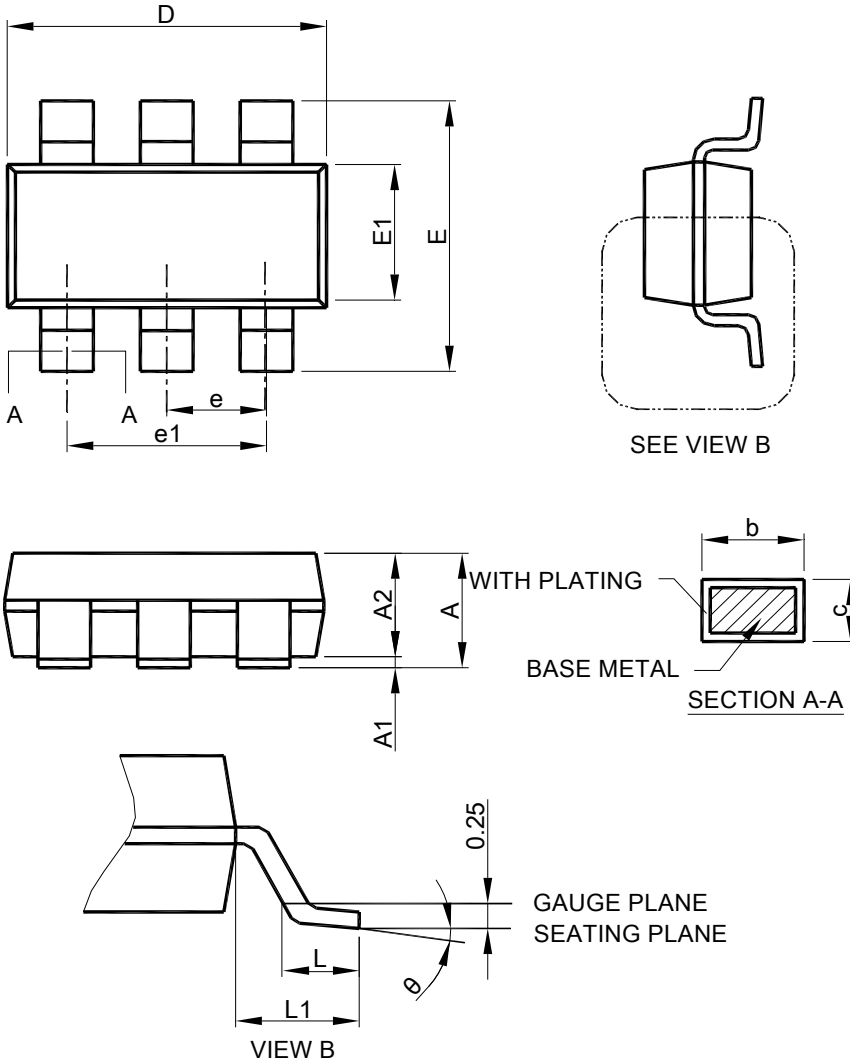


\*Note: Efficiency can boost if D1 is connected.

Fig.19 AIC3415 Application Circuit.

■ PHYSICAL DIMENSIONS

● SOT-23-6



SYMBOL	SOT-23-6	
	MILLIMETERS	
	MIN.	MAX.
A	0.95	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.30	0.50
c	0.08	0.22
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.70
e	0.95 BSC	
e1	1.90 BSC	
L	0.30	0.60
L1	0.60 REF	
$\theta$	0°	8°

- Note :
1. Refer to JEDEC MO-178AB.
  2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.
  3. Dimension "E1" does not include inter-lead flash or protrusions.
  4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

**Note:**

Information provided by AIC is believed to be accurate and reliable. However, we cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in an AIC product; nor for any infringement of patents or other rights of third parties that may result from its use. We reserve the right to change the circuitry and specifications without notice.

Life Support Policy: AIC does not authorize any AIC product for use in life support devices and/or systems. Life support devices or systems are devices or systems which, (i) are intended for surgical implant into the body or (ii) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.